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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHRIS E. BARNS, JUSTIN K. BRASK, and MARK DOCZY

Appeal 2009-001933
Application 10/629,127
Technology Center 2800

Decided: October 21, 2009

Before KENNETH W. HAIRSTON, KARL D. EASTHOM, and BRADLEY W. BAUMEISTER, *Administrative Patent Judges.*

Opinion for the Board filed by *Administrative Patent Judges* HAIRSTON and BAUMEISTER.

Opinion Dissenting-in-Part filed by *Administrative Patent Judge* EASTHOM.

BAUMEISTER, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal[1] under 35 U.S.C. § 134 from the Examiner's final rejection of claims 1-14, 16-19, and 25-28 (App. Br. 5). We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM-IN-PART.

Appellants' invention employs a hard mask 16 (Fig. 1), such as a nitride[2] hard mask, over a polysilicon gate structure 14 to aid in replacing the polysilicon gate with a metal gate. The mask protects the gate from silicides formed on other gate structures 14a. The mask is selectively etched. (Figs. 1-3; Abstract; Spec. 4-5).

Exemplary claims 1 and 14 follow:

1. A method comprising:

covering a polysilicon gate structure with a hard mask to prevent the formation of a silicide on the gate structure, said mask and said gate structure having opposed, common vertical surfaces; and

forming a sidewall spacer that extends along a vertical surface and covers said gate structure and covers at least part of said mask; and

removing said hard mask using an etch that is selective of the hard mask over the spacer.

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[1] Reference is made to Appellants' Brief (filed Jan. 3, 2006) ("App. Br.") and Reply Brief (filed May 11, 2006) ("Reply Br.") and the Examiner's Answer (mailed Mar. 28, 2006) ("Ans.") and Office Action Final Rejection (mailed Aug. 8, 2005) ("Fin. Rej.").

[2] We understand Appellants' use of the term "nitride" to be shorthand for "silicon nitride" (*see infra* pp. 12-13). Throughout this opinion, we likewise use the terms "silicon nitride" and "nitride" interchangeably.

14. A method comprising:

selectively preventing the formation of a silicide on a first polysilicon gate structure using a hard mask over said first polysilicon gate structure;

forming a silicide on a second polysilicon gate structure;

removing the hard mask using a selective etch; and

replacing the first polysilicon gate structure with a metal gate replacement.

The Examiner relies on the following prior art references:

Deckert	US 4,269,654	May 26, 1981
Yeh	US 5,023,694	Jun. 11, 1991
Wang	US 6,248,002 B1	Jun. 19, 2001
Lee '648	US 6,258,648 B1	Jul. 10, 2001
Lee '530	US 6,800,530 B2	Oct. 5, 2004 (filed Jan. 14, 2003)

The Examiner rejected:

Claims 1-3 and 5-12 as anticipated under 35 U.S.C. § 102(e) based on Lee '530;

Claim 13 as obvious under 35 U.S.C. § 103(a) based on Lee '530 and Wang;

Claims 4, 14, 16-19 and 25-27 as obvious under 35 U.S.C. § 103(a) based on Lee '648 and Lee '530; and

Claim 28 as obvious under 35 U.S.C. § 103(a) based on Lee '648, Lee '530, and Deckert.

ARGUMENTS AND ISSUES

Appellants' arguments focus on claims 1 and 14. Therefore, claim 1 is selected to represent claims 1-3 and 5-12, while claim 14 is selected to represent claims 14, 16-19, and 25-27. *See* 37 C.F.R. § 41.37(c)(1)(vii). As Appellants present no arguments for claims 4, 13, and 28 (App. Br. 9-13), the rejections of those claims are summarily sustained.

Claims 1-3 and 5-12

Relying on the manufacturing stages of Lee '530 that are depicted in Figures 7 and 8 and discussed in column 4 of the reference, the Examiner finds that the claimed hard mask reads on Lee's hard mask 52 and that the claimed sidewall spacer reads on Lee's etch stop layer 72 (Fin. Rej. 3). The Examiner further finds that the alternative processes disclosed for removing the hard mask 52, a chemical mechanical polishing (CMP) and a stripping process, are both inherently selective of hard mask 52 over sidewall spacer 72 (Ans. 3-4). The Examiner reasons that each of the processes removes the entire hard mask 52 while removing only the top portion of the sidewall layer 72 (Ans. 3-4). The Examiner further relies on column 17, lines 8-12, of Yeh to support the position that the stripping process inherently possesses a selective property (Fin. Rej. 3). We understand the Examiner, then, to be interpreting the term "selective etch" broadly to include an etch process that removes all of one layer or material and only a portion of another layer or material, regardless of the relative rates at which the process etches the two layers or materials.

Appellants argue, *inter alia*, that (1) "A selective etch is one that preferentially removes one type of material relative to another type of material" (Reply Br. 3); and (2) "There is no basis to conclude that Lee

necessarily uses a selective etch of the hard mask over the spacer" (App. Br. 10).

To support their arguments, Appellants present a modified version of Lee '530's Figure 7 in their Appeal Brief (App. Br. 17), reproduced below:

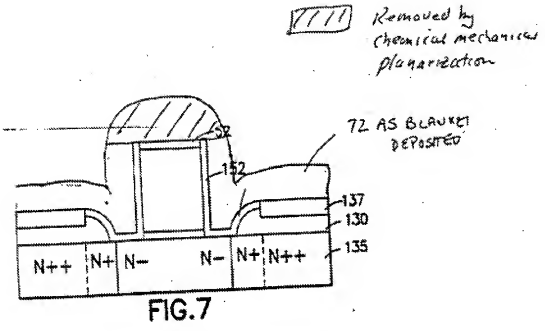

FIG.7

LEE '530 MODIFIED

The figure above (hereinafter "modified Figure 7") depicts Lee '530's gate structure within side walls 152 and 72, and under hard mask layer 52.

Appellants provide modified Figure 7 to show an implied (hatched) portion of sidewall spacer layer 72. This top (hatched) portion of sidewall layer 72 is not depicted in Lee '530, but Appellants explain (App. Br. 11) that Lee's blanket deposition process of forming the sidewalls 72 inherently forms this top portion of 72. That is, modified Figure 7 depicts a manufacturing stage that is subsequent to the stage depicted in Figure 7 of Lee '530 but prior to the stage depicted in Figure 8.

Appellants argue (App. Br. 11) that Lee '530 does not teach a selective etch because the CMP step of Lee's etch process not only removes the hard mask 52, but it also removes the implied (hatched) top portion of sidewall layer 72 above the mask:

> Thus, not only is the hard mask 52 removed, but a large portion of the layer 72 is removed, namely, the portion of the layer over and along the sides of the layer 52. Thus, there is no way to say that that mechanical polishing process is selective of the hard mask over the layer 72.

(App. Br. 11).

Appellants' arguments, then, raise the following issue with respect to the rejection of claims 1-3 and 5-12: Did Appellants demonstrate that the Examiner erred in finding that Lee '530 discloses "removing said hard mask using an etch that is selective of the hard mask over the spacer" as required by claim 1?

Claims 14, 16-19, and 25-27

Claim 14 recites *inter alia* using "*a* hard mask" to selectively prevent formation of a silicide on first gate structure, forming a silicide on a second gate structure, and removing "*the* hard mask" (emphasis added). The Examiner concludes that these features are disclosed by Lee '648. Specifically, the Examiner states:

> Lee '648 discloses in FIG. 2 to 6 a method comprising: selectively forming a nitride hard mask layer 26 on a first polysilicon gate structure 10; and forming a silicide 32 on a second polysilicon gate structure 10; and removing the hard mask 26 using a selectively [sic] etch (with a mask pattern 28 to form sidewall spacers 30).

(Fin. Rej. 5). The Examiner also states that claim 14 does not require removing the nitride hard mask 26 from over the first polysilicon gate

electrode, and "the limitation 'using a hard mask over said first polysilicon gate structure' does not necessarily preclude the hard mask to be formed on other structures" (Ans. 5).

We understand the Examiner's position to be, then, that by reciting "removing the hard mask using a selective etch," claim 14 only requires (1) that some portion of a previously formed hard mask needs to be removed—not the entire hard mask; and furthermore (2) that this removed portion may be removed from anywhere—not necessarily from over the first polysilicon gate structure. Under the Examiner's interpretation, Lee '648 teaches the first three limitations of claim 14 because even though Lee leaves unetched some portions of layer 26 so as to ultimately serve as sidewall spacer 30, Lee does etch some portions of the silicon nitride layer 26 from some regions of the gate structure of the second, Logic FET (Field Effect Transistor) 3.

Appellants alternatively argue *inter alia*:

> Claim 14 says that the first polysilicon gate structure is replaced with a metal gate replacement. Thus, the first polysilicon gate structure is fixed and defined in the claim. It must be the same first polysilicon gate structure that is the object of the phrase selectively preventing the formation of a silicide on the first polysilicon gate structure, it must be the one that gets the hard mask "over said first polysilicon gate structure," and the removing the hard mask step since it refers to "the hard mask" must be removing the hard mask over the first polysilicon gate structure. Logic permits no other reading of the claim.

(Reply Br. 3).

Appellants' arguments, then, raise the following issue with respect to the rejection of claims 14, 16-19, and 25-27: Did Appellants demonstrate that the Examiner erred in finding that Lee '530 and Lee '658 collectively

teach the limitation of claim 14, "removing the hard mask using a selective etch"?

FINDINGS OF FACT (FF)

1. Appellants attached a "definition of selective etch from the Internet glossary" (Reply Br. 2) at the end of their Reply Brief. The definition reads, "Selective Etch: Etching at unequal rates in limited areas, frequently caused by inhomogeneities in the workpiece material, hot spots from unequal heat transfer or, on a microscale, selected grain faces or constituents."

2. Lee '530 discloses a hard mask 50 comprising three sub-layers: "silicon nitride (Si3N4-nitride) 52 (30 nm thick), oxide 54 (15 nm thick), and a second or upper layer of nitride [56] (30 nm thick)" (col. 2, ll. 45-48). Lee '530 discloses etching the final layer of the stack, 52, in a two-step process as follows:

> A blanket deposition of a relatively thick layer of nitride 72 for an etch stop and oxide 76, for isolation of the conductive members in the local interconnect, forms a thick layer that is reduced by conventional chemical-mechanical polishing (CMP) to the level of the top of the gate stack. The final layer 52 of the hardmask may be polished away during this step, illustratively in a process that uses the exposure of poly 30 in the temporary gate as a signal to stop the polishing. If such a process is not used, the remaining portion of layer 52/152 is stripped, exposing the poly 30 in the gate.
>
> A poly etch removes gate 30, leaving an aperture lined with layer 152. Layer 152 may be left in place or stripped. . . . [A] new gate is deposited. The new gate may be chosen from a number of alternatives, such as Tungsten . . . . The new gate may preferably fill the aperture left by the old gate, though that is not required. It may be preferable . . . to fill the aperture partially and use the remaining space for a contact.

(Col. 4, ll. 9-38).

3. Yeh discloses completely etching away a previously patterned silicon nitride layer 106 and underlying regions of polysilicon layer 104 selectively relative to thermally oxidized regions 124 of polysilicon layer 104 as follows:

> The nitride layer 106 and oxide layer 108 together serve the purpose of defining a self-aligned paddle which helps reduce the cell size with a given design rule. If the self-aligned feature is not wanted, then the process can be simplified by implanting the paddle region with a mask before poly deposition. The poly can then be patterned directly with a mask, with a reverse tone to mask 114, without the deposition of nitride layer 106 and oxide layer 108 and the associated etching and oxidation steps.
>
> The next process step is to remove mask 118 and the underlying oxide layer 108 using a conventional etch. Thus, the nitride layer 106 remains to define the regions of the first and second portions of the first polysilicon layer. Referring now to FIG. 10, as seen in that figure, a second silicon dioxide layer 124 is thermally grown in a conventional manner on the exposed surface areas of the first polysilicon layer 104. Only an insignificant amount of oxide forms on the surface of nitride layer 106. The oxide layer 124 formed on the exposed surface areas comprises a masking oxide for the next step which is to complete the formation of the first and second portions of said first polysilicon layer 104.
>
> FIG. 11 illustrates the next step of the process, which is to strip the nitride layer 106 selectively with a wet etch and then use the oxide layer 124 as a mask for etching of the polysilicon layer 104 using a conventional anisotropic etch.

(Col. 16, l. 53 – col. 17, l. 12).

Lee '648

4. Lee '648 teaches forming a thick silicide protection layer 26 of silicon nitride over both a first gate structure 10 (in "Memory FET" 5) and a

second gate structure 10 (in "Logic FET" 3) (*see, e.g.*, col. 3, l. 65 – col. 4, l. 3; Fig. 3). A silicide blockout mask 28 serves as a nitride etch protection mask for the memory FET 5 (col. 4, ll. 3-5; Fig. 4). An anisotropic etch then partially removes the silicon nitride layer 26 from the unmasked region associated with Logic FET 3, leaving silicon nitride sidewall spacers 30 (Fig. 5, alternatively labeled as 34 in Fig. 6) on the gate sidewalls of the Logic FET 3 (col. 4, ll. 5-7; Figs. 5-6).

5. "The thick silicon nitride 26 silicide protection layer and nitride sidewall spacers 34, as shown in FIG. 6 are subsequently removed by selectively etching the nitride while leaving the oxide layers and salicide[3] layers intact" (col. 4, ll. 24-27). "In addition, after the salicide process is complete, said thick silicon nitride layer can be anisotropically etched to form sidewall spacers on the memory devices" (col. 4, ll. 53-55).

PRINCIPLES OF LAW

"[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). On appeal, the burden shifts to Appellants to overcome the prima facie case with arguments and/or evidence. *See id.*

Under § 102, anticipation is established when a single prior art reference discloses expressly or under the principles of inherency each and every limitation of the claimed invention. *In re Paulsen*, 30 F.3d 1475, 1478-79 (Fed. Cir. 1994). "A reference anticipates a claim if it discloses the

[3] We understand the term "salicide" to be shorthand for the term "self aligned silicide."

claimed invention 'such that a skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the invention.'" *In re Graves*, 69 F.3d 1147, 1152 (Fed. Cir. 1995) (quoting *In re LeGrice*, 301 F.2d 929, 936 (CCPA 1962) (emphasis omitted).

To establish prima facie obviousness of a claimed invention under § 103, all the claim limitations must be taught or suggested by the prior art. *See In re Royka*, 490 F.2d 981, 985 (CCPA 1974). "'[T]here must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.'" *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

During examination of a patent application, the PTO "is obligated to give claims their broadest reasonable interpretation during examination." *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1369 (Fed. Cir. 2004). "[T]he words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (citations omitted). "'[C]laims must be construed so as to be consistent with the specification, of which they are a part.'" *Id.* at 1316 (citation omitted).

"Judges are not like pigs, hunting for truffles buried in briefs." *SmithKline Beecham Corp. v. Apotex Corp.*, 439 F.3d 1312, 1320 (Fed. Cir. 2006).

ANALYSIS

I. Claims 1-3 and 5-12 –

Anticipation based on Lee '530

"Before considering the rejections . . ., we must first [determine the scope of] the claims . . . ." *In re Geerdes*, 491 F.2d 1260, 1262 (CCPA 1974). Accordingly, we must first determine the meaning of the language of claim 1, "removing said hard mask using an etch that is selective of the hard mask over the spacer." That is, we must first determine whether an etching process may be deemed to be selective (1) only if, as Appellants urge, the process etches two materials at different rates; or alternatively, and in accordance with the Examiner's broader interpretation, (2) if the process merely etches two materials at any relative rate, including at the same rate, but leaves remaining a portion of one of the two materials.

To evidence that the narrower interpretation is the proper one, Appellants have made of record a web page of the Photo Chemical Machining Institute (*see* Reply Br. 3). This web page includes a glossary of terms and definitions including the following definition of a selective etch: "Etching at *unequal rates* in limited areas, frequently caused by inhomogeneities in the workpiece material, hot spots from unequal heat transfer or, on a microscale, selected grain faces or constituents" (FF 1 (emphasis added)). Conversely, the Examiner has provided no evidence on the record to support the Examiner's alternative, broader interpretation of the term "selective etch." Accordingly, we find that an etch process must etch two materials at different rates in order to be deemed to be a selective etch.

Turning to the art applied against claim 1, Lee '530 discloses that hard mask layer 50 comprises three sublayers: "silicon nitride (Si3N4-nitride) 52

(30 nm thick), oxide 54 (15 nm thick), and a second or upper layer of nitride [56] (30 nm thick)" (FF 2). We understand the expression "silicon nitride (Si3N4-nitride) 52" to mean that the terms "Si3N4" and "nitride" are both synonymous with the term "silicon nitride." This interpretation is supported by the subsequent reference in Lee to the "second or upper layer of nitride" 56 (FF 2). That is, by setting forth that the first, lowermost layer 52 is composed silicon nitride and the third, uppermost layer 56 is a "second . . . layer of nitride," Lee indicates that "nitride" is synonymous with "silicon nitride."

Lee '530 further discloses that etch stop layer 72 is also composed of a nitride (FF 2). The Examiner has not asserted any contrary positions (*see* Ans. 3-4). We therefore next inquire whether there is any evidence of record indicating that one layer of silicon nitride (hard mask 52) can be selectively etched relative to another layer of silicon nitride (etch stop 72).

The Examiner acknowledges that Lee '530 does not expressly state that the CMP or stripping process used to remove hard mask 52 is selective of the hard mask relative to the etch stop 72 (*see* Fin. Rej. 3; Ans. 3-4). Accordingly, the Examiner relies on column 17, lines 8-12, of Yeh for a discussion of "[such an] inherent selective property of the stripping process toward the nitride hard mask" (Fin. Rej. 3). However, Yeh does not teach that one layer or region of silicon nitride may be selectively etched relative to another layer or region of silicon nitride. Rather, the passage of Yeh relied upon by the Examiner discloses completely etching away a previously patterned silicon nitride layer 106 in combination with underlying regions of polysilicon layer 104. This complete etch of silicon nitride is selective relative to thermally oxidized regions 124 of polysilicon layer 104 (FF 3).

As such, the Examiner has not provided any evidence on the record that the silicon nitride hard mask 52 of Lee '530 is selectively etched relative to silicon nitride etch stop 72.

Accordingly, Appellants have persuaded us of error in the Examiner's anticipation rejection of representative claim 1. We therefore reverse the Examiner's decision rejecting that claim and dependent claims 2, 3, and 5-12, which fall with claim 1.

II. Claims 14, 16-19, and 25-27 –

Obviousness based on Lee '648 and Lee '530

Before addressing the merits of the rejection, we first determine the meaning of the claim 14 limitations, "selectively preventing the formation of a silicide on a first polysilicon gate structure using *a* hard mask over said first polysilicon gate structure" and "removing *the* hard mask using a selective etch" (claim 14 (emphasis added)). *See Geerdes*, 491 F.2d at 1262. In so doing we specifically note that the use of the article "a" in the limitation "selectively preventing [silicide] using a hard mask . . . " and the use of the article "the" in the subsequent limitation "removing the hard mask using a selective etch" are highly significant.

By reciting "using *a* hard mask" (instead of other potential language such as "using hard mask material"), claim 14 indicates that the entire hard mask pattern that resides over the first polysilicon gate structure must be viewed as a single unit. Furthermore, by reciting "removing *the* hard mask . . . " (instead of other potential language such as "removing hard mask material) claim 14 indicates that (1) the hard mask that is being removed in the third claim step is the same hard mask pattern or unit that was employed over the first polysilicon gate structure, and (2) the entire hard mask pattern

unit must be removed. This interpretation is consistent with the plain meaning of the claim language and also consistent with Appellants' usage within the Specification (*see* Spec. 4-7; Figs. 4-5).[4]

Turning to the art applied against claim 14, Lee '648 discloses that a thick silicide protection layer 26 of silicon nitride is formed over both a first gate structure 10 (in "Memory FET" 5) and a second gate structure 10 (in "Logic FET" 3) (FF 4). A silicide blockout mask 28 serves as a nitride etch protection mask for the memory FET 5 (*id.*). An anisotropic etch partially removes the silicon nitride layer 26 from the uncovered, Logic FET 3 region, leaving silicon nitride sidewall spacers 30/34 (Figs. 5-6) on the gate sidewalls of the Logic FET 3 (FF 4). Lee '648 further discloses that the thick silicon nitride silicide protection layer 26 may subsequently be completely removed from over the first, Memory FET 5 by using a selective etch (FF 5). Alternatively, the silicon nitride layer 26 may be partially removed by means of an anisotropic etch so as to form sidewall spacers on the first, Memory FET (*id.*).

The Examiner, though, does not base the obviousness rejection upon Lee's teaching of removing the nitride layer 26 from Lee's *Memory FET 5* (or "first polysilicon gate structure") (*see* Fin. Rej. 5-6; Ans. 4-5). Rather, the Examiner bases the rejection on the fact that Lee removes a portion of

[4] To clarify, we do not reach the question of whether claim 14 requires removing the entirety of every individual mask pattern 26 produced anywhere on a semiconductor substrate from an initially deposited single layer of hard mask material. But for the reasons set forth above, we do find that claim 14 requires removing at least the entirety of the particular mask pattern that is disposed over the first polysilicon gate structure.

the silicide protection layer 26 from a portion of Lee's *Logic FET 3* (or "second polysilicon gate structure"):

> Lee '648 discloses in FIG. 2 to 6 a method comprising: selectively forming a nitride hard mask layer 26 on a first polysilicon gate structure 10; and forming a silicide 32 on a second polysilicon gate structure 10; and removing the hard mask 26 using a selectively [sic] etch (with a mask pattern 28 to form sidewall spacers 30).

(Fin. Rej. 5). In so doing, the Examiner also appears to be somehow viewing method claim 14's process step of "selectively preventing the formation of a silicide on a first polysilicon gate structure using a hard mask over said first polysilicon gate structure" as an intended use within an apparatus claim:

> Re further claims 14 and 16-19, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed ("selectively preventing the formation of a silicide on a first polysilicon gate structure ", etc.) does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex Parte Masham*, 2 USPQ F. 2d 1647 (1987).

(Fin. Rej. 6).

The Examiner proceeds to admit that "Lee '648 fails to disclose replacing the first polysilicon gate structure with a metal gate replacement" (Fin. Rej. 5). The Examiner notes though that "Lee '530 suggests in FIG. 8 replacing a polysilicon gate structure 30 with a metal gate replacement 133, and removing mask 52 after forming a silicide 137" (Fin. Rej. 6). Then without any further explanation, the Examiner summarily concludes: "It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Lee '648 as suggested by Lee

'530 because of the desire to form a temperature sensitive gate electrode so as to enhance device performance" (*id.*).

The rejection is so brief and sketchy that it does not explain if Lee '530 is being relied upon only for the replacement of the Memory FET's polysilicon gate with a metal gate, or alternatively if the silicided source and drain of Lee '530 are also being incorporated into the Memory FET 5 of Lee '648. The rejection does not explain if the gate of Logic FET 3 in Lee '648 is to remain silicided, or alternatively, if the silicided gate is to be subsequently replaced with a metal gate as well. The rejection does not explain whether the thick nitride layer 26 of Lee '648 somehow corresponds to the nitride blanket 72 of Lee '530, or alternatively, whether one of these two layers is first deposited and removed prior to forming the other of the two layers. Most notably missing, the rejection does not set forth whether the nitride hard mask 52 of Lee '530 is to be deposited on the Memory FET 5 of Lee '648 prior to siliciding Logic FET 3.

Restated, the rejection is devoid of any substantive explanation of (1) what process steps of Lee '530 are being incorporated into the manufacturing process of Lee '648, (2) how the process of Lee '648 is being modified, or (3) what final structures are to be produced by the process of Lee '648 when modified by Lee '530. In short, the rejection is simply too incomplete to conclude with any reasonable degree of confidence what the Examiner's position is. As such, the Examiner cannot be said to have met the initial burden of establishing a prima facie showing of obviousness. Therefore, the burden of rebuttal has not shifted to Appellants. *See Oetiker*, 977 F.2d at 1445.

The dissent finds that even if claim 14 does require total mask removal, the combination of Lee '648 and Lee '530 suggests the total removal of a hard mask from over the Memory FET 5 of Lee '648 because (1) Lee '530 necessarily forms a thin mask 52 prior to the thicker mask layer 72; and (2) Lee '530 teaches the total removal of the thin mask 52 from over a gate (Dissent 1-4). That is, the Dissent finds that all of the limitations of claim 14 would necessarily be taught if Lee '648 were modified so as to form the thin mask 52 of Lee '530 over the Memory FET 5 and subsequently remove the mask (*id.*).

However, the plain language of the Examiner's Final Rejection and Answer indicates that this was not the rationale upon which the Examiner based the rejection (*see* Fin. Rej. 5-6; Ans. 4-5). Moreover, the dissent's theory is premised on the speculative assumption that the manufacturing process of Lee '648 is to be modified such that thin mask 52 of Lee' 530 is deposited on Memory FET 5 *prior* to the siliciding of Logic FET 3. In fact, the Examiner never asserted this, and it is possible to combine the two Lee references and achieve various structures through manufacturing processes where the thin mask 52 is formed *after* siliciding Logic FET 3. For example, the manufacturing process of Lee '648 could be followed unaltered through the stage depicted in Figure 6; thick mask pattern 26 – which protected the memory FET during the siliciding process – could then be *partially* removed after siliciding the Logic FET; and then thin mask 52 could be placed over the gate of the Memory FET for the purpose of protecting that gate – not the gate of the other, Logic FET – during a subsequent step of siliciding the source/drain regions of the Memory FET.

In short, the dissent's alternative rationales for sustaining the finding of obviousness are tantamount to wholly new grounds of rejection. *But see Ex parte Gambogi*, 62 USPQ2d 1209, 1211 (BPAI 2001) (noting that the Board of Patent Appeals and Interferences "is basically a board of review– we review . . . rejections made by patent examiners"). Since no such rationales or associated arguments were raised on appeal, we find it imprudent to speculate *ab initio* on alternative ways in which the two Lee references might be capable of being combined.[5] Judges are not like pigs, hunting for truffles buried in prior-art references. *See SmithKline Beecham*, 439 F.3d at 1320.

Accordingly, Appellants have persuaded us of error in the Examiner's obviousness rejection of representative claim 14. For the foregoing reasons then, we reverse the Examiner's decision rejecting method claim 14 and dependent claims 16-19 and 25-27, which fall with claim 14.

CONCLUSION

I. Appellants have demonstrate that the Examiner erred in finding that Lee '530 discloses "removing said hard mask using an etch that is selective of the hard mask over the spacer" as required by claim 1. As such, Appellants have shown that the Examiner erred in rejecting claims 1-3 and 5-12 under 35 U.S.C. § 102.

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[5] Too many unanswered questions exist for this tribunal to now propose new rationales for combining the Lee references. For example, the dissent's proposed rationale raises the question of whether performing a CMP to remove the nitride layer 52 (of Lee '530) from the Memory FET 5 (of Lee '648) would destroy the silicide layer that was previously formed on the gate of Logic FET 3 (of Lee '648).

II. Appellants have demonstrated that the Examiner erred in finding that the cited prior art collectively teaches or suggests the limitation of claim 14, "removing the hard mask using a selective etch." As such, Appellants have shown that the Examiner erred in rejecting claims 14, 16-19, and 25-27 under 35 U.S.C. § 103.

III. Appellants have not presented any arguments in relation to the Examiner's rejections of claims 4, 13, and 28. As such, Appellants have not shown that the Examiner erred in rejecting claims 4, 13, and 28 under 35 U.S.C. § 103.

DECISION

We reverse the Examiner's decision rejecting claims 1-3, 5-12, 14, 16-19, and 25-27.

We summarily affirm the Examiner's decision rejecting claims 4, 13, and 28.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

EASTHOM, *Administrative Patent Judge*, DISSENTING-IN-PART.

I join with the majority opinion as summarized *supra* in CONCLUSION Sections I and III, and respectfully DISSENT with respect to CONCLUSION Section II. For the reasons that follow, I would affirm the Examiner's decision to reject claims 14, 16-19, and 25-27.

My understanding of the Examiner's position with respect to claim 14 differs with that of the majority. I understand that the Examiner's position requires removing the mask over the first gate electrode in Lee '648 because there is no other way for the material under that mask to be replaced according to the Examiner's rejection (in reliance on the teachings of Lee '530). The majority does not address this position, advanced in the Examiner's rejection as outlined below. Rather, the majority reasons that the Examiner's position is that the mask 26 portion of Lee '648 over the first gate need not be removed (an errant claim interpretation imputed to the Examiner). In addition, the majority implies that even if the record teaches that some mask portion over the first gate of Lee '648 is removed, claim 14 requires removal of whatever mask material was initially deposited in the vicinity of the first gate, including portions not over the first gate (*see supra* note 4).

While I do not agree with this claim interpretation,[1] resolving the issue is not required, since it appears that the majority finds that Lee '648 teaches whatever mask removal the claim requires.

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[1] Appellants do not argue that claim 14 requires removing the whole mask 26 of Lee '648. "It is the applicants' burden to precisely define the invention, not the PTO's." *In re Morris*, 127 F.3d 1048, 1056 (Fed. Cir.

In addition, as discussed below and as noted by the Examiner (Fin. Rej. 5), Lee '530 also teaches total removal of a small mask 52 over a gate. This Lee '530 mask 52, necessarily formed prior to (i.e., under) the Lee '530 nitride mask layer 72, would have likewise been formed under the Lee '648 nitride mask layer 26, thereby also suggesting the argued claim limitation.

The Examiner found, as Appellants and the majority acknowledge (*see* App. Br. 12; Maj. Op. 6), that Lee '648 teaches the first three steps of claim 14 including the disputed limitations of forming "a hard mask over said first polysilicon gate structure" and "removing the hard mask." With respect to these first three steps of claim 14, the Examiner stated:

> Lee '648 discloses in FIG. 2 to 6 a method comprising: selectively forming a nitride hard mask layer 26 on a first polysilicon gate structure 10; and forming a silicide 32 on a second polysilicon gate structure 10; and removing the hard mask 26 using a selectively [sic] etch (with a mask pattern 28 to form sidewall spacers 30).

(Fin. Rej. 5).

The Examiner "modif[ied] the process of Lee '648 as suggested by Lee '530" (Fin. Rej. 6) to teach the final claim step, finding that "Lee '530 suggests in FIG. 8 replacing a polysilicon gate structure 30 with a metal gate replacement 133, *and removing mask 52 after forming a silicide* 137" (*id.* (emphasis added)).

1997). Appellants not only did not argue this claim interpretation of total mask removal, but disavowed it. "Certainly 'the' hard mask that is referred to in the third clause is the only hard mask in the claim. That is the hard mask over the first polysilicon gate electrode" (App. Br. 12; *accord* Reply Br. 3). Removing a mask only over the gate structure is consistent with the Specification (*compare* Fig. 1 *with* Fig. 2).

In other words, the Examiner found that Lee '530 teaches not only the final claim step requiring metal gate replacement, but also teaches totally removing mask 52 over that gate structure – an essential pre-requisite step to replacing (with metal) the polysilicon under that first gate (i.e., suggesting the removal of either Lee '648's mask 26 (over the first gate) and/or Lee '530's similar mask 52). No dispute exists that, as Lee '530's mask 52 resides only over the gate structure which it protects, its subsequent removal is also total, as Lee '530 teaches. (*See, e.g.*, Lee '530's modified Figure 7 and discussion *supra* with respect to claim 1.)

Further, no dispute exists that Lee '648's mask 26 must be removed over the first (Memory) gate in order to combine Lee '530's teaching of metal replacement in that gate, and that Lee '648 teaches totally removing the remaining mask portions 26 as a last optional step. The majority implicitly reasons that the Examiner and Appellants lacked this common understanding because the Examiner made an errant claim interpretation[2] and did not specifically spell out these common understandings fully detailed in the two references cited. The majority then concludes that the dissent's explicit statements concerning this rejection amount to a new rejection.

[2] A close reading of the Examiner's rejection and reasoning, quoted above (Maj. Op. 16-17), reveals no specific statement that "[t]he Examiner also states that claim 14 does not require removing the nitride hard mask 26 from over the first polysilicon gate electrode" as the majority contends (Maj. Op. 6-7). As such, the Examiner reasonably could have simply meant that the claim does not preclude removing other portions of the gate 26 in addition to those portions over the gate. Or, the Examiner could have erred in determining that the claim only requires some mask removal away from the first gate. As discussed below, the latter determination necessarily conflicts with the thrust of the rejection and as such, must be an alternative theory.

However, there is nothing new in the idea that the mask over the gate must be removed to remove the material under the gate. As quoted *supra*, the Examiner stated that Lee '530 teaches "*removing mask 52 after forming a silicide* 137." (Of course the mask must be formed before it is removed.) The Examiner, and Appellants, as skilled artisans armed with common knowledge, understood the thrust of this rejection. "'Our suggestion test is in actuality quite flexible and not only permits, but requires, consideration of common knowledge and common sense.'" *KSR*, 550 U.S. at 421 (citation omitted) (emphasis omitted).

Therefore, even if the Examiner erred as to claim construction by reasoning that other portions of the mask 26 could be removed to satisfy the claim (*but see supra* Dissent note 2), the thrust of the rejection calls for removing any portion of any mask (including the Lee '648 mask 26) protecting the gate. At most, the Examiner's supposedly errant claim construction constitutes an alternative theory to the underlying rejection, a rejection which remains un-rebutted, or, at least, persuasive.

While the majority correctly notes that judges should not search for "truffles" in the Briefs (Maj. Op. 19 (citing *SmithKline Beecham*, 439 F.3d at 1320)), the majority, without any argument by Appellants, ironically envisions and details a myriad of potential problems with the mask removal outlined in the "brief and sketchy" rejection (*supra* note 5; Maj. Op. 17).[3]

[3] Despite the majority concerns with CMP mask removal (*supra* note 5), the record is not so limited: Lee '530 uses a stripping process to remove the mask 52, Lee '648 removes the nitride mask 26 without concern over destroying adjacent silicide structures, and skilled artisans would have recognized other selective removal techniques, including, for example, a

The majority approach improperly shifts the burden. Even if the Examiner's rejection were "sketchy" enough to constitute an error in the prima facie case, on appeal, Appellants have the burden to point to any such error. *See Oetiker*, 977 F.2d at 1445. At that point, the Examiner would have had the option of re-opening prosecution, or, in the Answer, possibly filling in any missing gaps in the puzzle pieces. "Common sense teaches, however, that . . . a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR*, 550 U.S. at 420.

Notwithstanding the majority concerns about "too many unanswered questions" (*supra* note 5), Appellants only argue that the claim calls for removing the mask over the gate. There is no dispute that each reference teaches that limitation, and the record shows that the Examiner stated so (stating that Lee '648 teaches the first three claim steps and that Lee '530 teaches mask 52 removal). The majority focuses on an Examiner response to Appellants' argument that is not germane to the rejection. Appellants did not even generally argue that the claim steps as set forth in the proposed combination would have been "uniquely challenging or difficult for one of ordinary skill in the art." *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007) (citation omitted).

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selective etch technique, so well known as to be defined in a standard reference, as found *supra* with respect to claim 1.

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